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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,760	12/26/2001	John F. Zumkehr	219.40219X00	1662

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,760	ZUMKEHR, JOHN F.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 remain in the application and have been examined.

Drawings

Figure 4 is objected to because the elements of the figure are too dark to distinguish the labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 5-9, 11, 13-16, 23, 25, 27 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by McCord (US-2003/0076125), hereinafter McCord.

Claims 1, 7-9, 15, 16, 23, and 27:

"a pattern generating device to generate a clock test pattern and a data test pattern"

McCord teaches that sequencer 100 is coupled to CPU 30 by a communication interface 102 through which sequencer 100 receives test parameters, test data, correct test results, and test procedures, which are stored by sequencer 100 in random access memory (RAM) 104. McCord also teaches sequencer 100 is further connected to a DDR memory controller 236, which controls DUT 14 through relays 92 and connector 22.

"buffer devices to receive said clock test pattern and said data test pattern"

McCord teaches DDR memory controller 236 may further be coupled to optional DDR memory devices 243, which permit test instructions, test data, and/or test results

to be buffered by DDR memory controller 236 before transfer to sequencer 100 for storage in RAM 104.

"a pattern checking device to check patterns received from said buffer devices"

McCord teaches in response to receipt of test results from DUT 14, sequencer 100 logs the test results in RAM 104 and compares the test results with correct results also stored in RAM 104 to make a pass/fail determination for DUT 14.

"clock generating logic to control a clock for said clock test pattern and a clock for said data test pattern"

McCord teaches communication between DDR memory controller 236 and DUT 14 is synchronized by timing signals based upon controller clocks 120, which are received by DDR memory controller 236. McCord also teaches controller clocks 120 are selected by selector 124 (as per claims 7, 15 and 27) from among a plurality of clock signals generated by clock sources 122 in response to a clock select signal 38 (as per claims 8 and 16) output by CPU 30. (Pages 3-4, ¶s 62-65).

Claims 3, 11, and 25:

"said test mode comprises an AC I/O loopback test"

McCord teaches during testing, sequencer 100 sets AC test parametrics for DUT 14, initiates READ and WRITE data transfers to and from DUT 14, and issues commands for DUT 14 based upon the test information stored in RAM 104. McCord also teaches in response to receipt of test results from DUT 14, sequencer 100 logs the

test results in RAM 104 and compares the test results with correct results also stored in RAM 104 to make a pass/fail determination for DUT 14. (Page 4, ¶ 64).

Claims 5 and 13:

McCord teaches said buffer devices are provided within a memory controller. (Page 4, ¶ 63). Also refer to the rejection of claims 1, 9 and 23 above.

Claims 6, 14 and 28:

"clock generating logic includes a delay element"

McCord teaches in order to test the timing sensitivity of DUT 14, DQS signals 242 and 244 are among the signals passed through respective sets of programmable delays 238 and 240, which applies a delay specified by a respective one of tester logic (TL) delay signals 40 and DUT delay signals 42. (Page 4, ¶ 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 4, 10, 12, 17-22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCord (US-2003/0076125), hereinafter McCord, in view of Kanda et al. (US-6671787), hereinafter Kanda.

Claim 17:

"A clock generating circuit to generate a first clock signal and a second clock signal for a DDR device,"

McCord teaches communication between DDR memory controller 236 and DUT 14 is synchronized by timing signals based upon controller clocks 120, which are received by DDR memory controller 236. McCord also teaches controller clocks 120 are selected by selector 124 from among a plurality of clock signals generated by clock sources 122 (first and second clocks) in response to a clock select signal 38 output by CPU 30. (Page 4, ¶ 65).

McCord does not explicitly teach "**said clock generating circuit generates said first clock signal in phase with said second clock signal when in a test mode and generates said first clock signal out of phase with said second clock signal when in a normal mode**". However, McCord does teach, as disclosed above, a plurality of clock signals generated by clock sources 122 (first and second clocks) in response to a clock select signal 38 (normal mode or test mode). Kanda teaches clock buffer 16 generates a clock signal CLK0° (in phase) in synchronization with the rising edge of the external clock signal CLK, while it generates a clock signal CLK180° (out of phase) in synchronization with the falling edge of the external clock signal CLK. (Col. 9, ll. 2-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify McCord's clock sources 122 to include Kanda's teaches clock buffer 16.

The artisan would have been motivated to do so because it would explicitly enable McCord's clock sources 122 to generate CLK0° (in phase) and CLK180° (out of phase) clocks to properly test the DDR device selected by selector 124.

Claims 2, 10, and 24:

"said clock generating logic operates such that in a test mode the clock for the clock test pattern is in phase with said clock for said data test pattern"

This claim limitation is rejected as per claim 17 above.

Claims 4, 12, and 26:

"said clock generating logic operates such that in a normal mode, said clock for said clock test pattern is out-of-phase with said clock for said data test pattern"

These claims are rejected as per claim 17 above.

Claim 18:

"said test mode comprises an AC I/O loopback test"

McCord teaches during testing, sequencer 100 sets AC test parametrics for DUT 14, initiates READ and WRITE data transfers to and from DUT 14, and issues commands for DUT 14 based upon the test information stored in RAM 104. McCord also teaches in response to receipt of test results from DUT 14, sequencer 100 logs the test results in RAM 104 and compares the test results with correct results also stored in RAM 104 to make a pass/fail determination for DUT 14. (Page 4, ¶ 64).

Claim 19:

McCord teaches said buffer devices are provided within a memory controller. (Page 4, ¶ 63). Also refer to the rejection of claims 1, 9 and 23 above.

Claim 20:

"clock generating circuit includes a delay element"

McCord teaches in order to test the timing sensitivity of DUT 14, DQS signals 242 and 244 are among the signals passed through respective sets of programmable delays 238 and 240, which applies a delay specified by a respective one of tester logic (TL) delay signals 40 and DUT delay signals 42. (Page 4, ¶ 65).

Claims 21 and 22:

McCord teaches controller clocks 120 are selected by selector 124 (as per claim 21) from among a plurality of clock signals generated by clock sources 122 in response to a clock select signal 38 (as per claim 22) output by CPU 30. (Page 4, ¶ 65).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Nakano et al. (US-6397312)

Nakano Teaches phase shifted clock generation incorporating delay elements (DLL circuits 41 and 51) and switching between these phases utilized in a DDR-SDRAM. (Claims 1, 2, 4, 6-9, 17 and 23).

b. Yoshimura et al., (A Delay-Locked Loop and 90-degree Phase Shifter for 100 Mbps Double Data Date Memories)

Yoshimura teaches 90-degree phase shifter utilized in a DDR-SDRAM. (Claims 1, 2, 4, 6-9, 17 and 23).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

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